

REMARKS

Applicants appreciate the Examiner's thorough review of the present application, and respectfully request reconsideration in light of the preceding amendments and the following remarks.

Claims 1-4 and 11-20 are pending in the application. Claims 5-10 have been cancelled without prejudice or disclaimer. Claims 1 and 11 have been amended only to improve claim language without otherwise touching the merits. Claims 12-20 have been added to provide Applicants with the scope of protection to which they are believed entitled. The Abstract has been amended to be compliant with commonly accepted US patent practice. No new matter has been introduced through the foregoing amendments.

The Office Action does not include a copy of the PTO-1449 submitted with the information disclosure statement filed December 10, 2001. Applicants respectfully request that the information submitted in the above identified IDS be considered and a copy of the PTO-1449, with the Examiner's initial(s) placed adjacent to the citation(s) on the PTO-1449, be returned to Applicants' representative in the next office communication.

The Examiner's acknowledgement of the priority claim and receipt of the certified copy of the priority document submitted December 10, 2001 is respectfully requested.

The claim objection is believed overcome in view of the above amendments.

The *35 U.S.C. 103(a)* rejections of claims 1-11 as being unpatentable over *Grigg* (U.S. Patent No. 6,506,681) is traversed, because the reference clearly fails to teach or suggest all limitations of the rejected claims.

The characteristic feature of the present invention is that the ultraviolet tape attached to a first surface of a wafer is irradiated with ultraviolet light to relieve the adhesive stress prior to a

lapping procedure, and the first surface of the wafer is placed on a lapping jig with the ultraviolet tape attached thereto, and the binder is applied to an upper surface of the lapping jig, then the first side of the wafer is bonded to the lapping jig via the binder, wherein the temperature of the lapping jig is controlled within a usable temperature range of the ultraviolet tape that causes the binder to melt, but is lower than the deformation temperature of the ultraviolet tape, thereby preventing deformation of the ultraviolet tape.

The object of the invention is to provide a process of lapping a wafer, which can overcome the problems caused by inherent adhesive stress and wafer deformation caused by the condition of the lapping jig. The present invention also overcomes the problem of the prior art where ultraviolet tapes can be used only for wafer grinding, but cannot be used for wafer lapping. In accordance with the present invention, UV tapes can now be used for wafer lapping.

Grigg fails to render the invention of independent claims 1 and 11 obvious for the following reasons.

First, *Grigg* fails to teach or suggest the claimed **lapping** step. See claim 1, line 3 from bottom and claim 11, line 4 from bottom. The *Grigg* patent in the portions cited by the Examiner teaches only grinding. Lapping and grinding are completely different processes as defined in the present specification (the paragraph bridging pages 7-8) and widely understood in the art (see, for example, the highlighted portions of attached Exhibit A and Exhibit B). Accordingly, the Examiner's statement that *Grigg* discloses lapping in page 1, lines 12-13 from bottom of the Office Action, is erroneous and should be withdrawn.

Second, *Grigg* clearly fails to teach or suggest **both** the claimed **UV tape and binder**. See claim 1, lines 4 and 9, and claim 11, lines 3 and 12. The unique feature of the present invention of using both UV tape and binder in wafer processing in order to simplify the manufacturing process and minimize wafer damages is not disclosed or suggested in the applied reference. *Grigg* teaches

using UV tape or binder. See column 2, lines 43-44 (i.e., protective member or submount), lines 47-49 (i.e., protective member can be UV tape whereas submount can be wax). Thus, according to *Grigg*, UV tape and binder are to be used as alternatives. The reference does not teach or suggest using UV tape and binder together in the presently claimed manner.

For the above reasons, it is believed that independent claims 1 and 11 are patentable over *Grigg*. Claims 2-4 depending from claim 1 and should be considered patentable for at least the same reasons. Claims 2-4 are also patentable on their own merits since these claims recite other features of the invention neither disclosed, taught nor suggested by the applied art.

As to claim 2, the Examiner has not demonstrated how the claimed step of **placing the lapping jig on a hot plate for a predetermined period of time** is disclosed or suggested by *Grigg* or the knowledge generally available in the art. Clarification is respectfully requested.

As to claim 3, the Examiner has not demonstrated how the claimed **Aqua wax** is disclosed or suggested by *Grigg* or the knowledge generally available in the art. Clarification is respectfully requested.

As to claim 4, the Examiner has not demonstrated how the claimed **temperature range** is disclosed or suggested by *Grigg* or the knowledge generally available in the art. Clarification is respectfully requested.

Applicants respectfully submit that the 35 U.S.C. 103(a) rejections of claims 1-11 as formulated by the Examiner are inappropriate and should be withdrawn.

New claims 12-14 depend from claim 1, and are considered patentable at least for the reason advanced with respect to claim 1. Claims 12-14 are also patentable on their own merits since these claims recite other features of the invention neither disclosed, taught nor suggested by the applied art.

As to claims 12-13, the applied reference fails to disclose, teach or suggest that **said irradiating step is performed before said lapping step**, as recited in claim 12. The Examiner's argument in page 2, lines 4-9 from bottom of the Office Action is noted. Applicants respectfully disagree with the Examiner's holding that it would have been obvious to irradiate the UV tape of *Grigg* before grinding. In column 3, lines 1-11 of the '681 patent, *Grigg* discloses that it has been known in the art, e.g., from U.S. Patent No. 6,030,485 to *Yamada*, to irradiate UV tapes with UV rays in the drying process, thereby allowing the UV tapes to be peeled off. It is well understood in the art that drying is conducted after wafer grinding. *See*, for example, the highlighted portions of attached Exhibit C. Thus, *Grigg* as well as the knowledge generally available in the art only teach irradiating the UV tapes after wafer grinding. In contrast, the method of claims 12-13 requires irradiating the UV tapes **before** wafer lapping. Claims 12-13 are thus patentable over the art.

As to claim 13, the applied reference fails to disclose, teach or suggest that **said irradiating step is performed before said bonding step**.

As to claim 14, the applied reference fails to disclose, teach or suggest that, in said bonding step, **the ultraviolet tape is bonded to the lapping jig via the binder**, at least because the art fails to teach or suggest using UV tape and binder together. *See* also Fig. 1e of the instant application.

New claims 15-17 depend from claim 11, and are considered patentable at least for the reason advanced with respect to claim 11. Claims 15-17 are also patentable on their own merits since these claims recite other features of the invention neither disclosed, taught nor suggested by the applied art, as discussed above with respect to claims 12-14, respectively.

New independent claim 18 is patentable over the applied art of record at least for the reason advanced with respect to claim 12.

New claims 19-20 depend from claim 18, and are considered patentable at least for the reason advanced with respect to claim 18. Claims 19-20 are also patentable on their own merits

since these claims recite other features of the invention neither disclosed, taught nor suggested by the applied art, as discussed above with respect to claims 13-14, respectively.

Each of the Examiner's rejections has been traversed. Accordingly, Applicants respectfully submit that all claims are now in condition for allowance. Early and favorable indication of allowance is courteously solicited.

The Examiner is invited to telephone the undersigned, Applicant's attorney of record, to facilitate advancement of the present application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

LOWE HAUPTMAN GILMAN & BERNER, LLP



Benjamin J. Hauptman
Registration No. 29,310

USPTO Customer No. 22429
1700 Diagonal Road, Suite 310
Alexandria, VA 22314
(703) 684-1111 BJH/KL/klb
(703) 518-5499 Facsimile
Date: January 7, 2004

Exhibit A



US006672943B2

(12) United States Patent Vogtmann et al.

(10) Patent No.: US 6,672,943 B2
(45) Date of Patent: Jan. 6, 2004

(54) ECCENTRIC ABRASIVE WHEEL FOR
WAFER PROCESSING

(75) Inventors: Michael Vogtmann, Pleasanton, CA
(US); Krishna Vepa, Livermore, CA
(US); Michael Wisnieski, Pleasanton,
CA (US)

(73) Assignee: Wafer Solutions, Inc., Fremont, CA
(US)

(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/845,710

(22) Filed: Apr. 30, 2001

(65) Prior Publication Data

US 2002/0102920 A1 Aug. 1, 2002

Related U.S. Application Data

(60) Provisional application No. 60/264,569, filed on Jan. 26,
2001.

(51) Int. Cl.⁷ B24G 1/00

(52) U.S. Cl. 451/41; 451/259; 451/287;
451/548

(58) Field of Search 451/41, 64-66,
451/259, 270, 287-291, 397, 398, 402,
540, 548, 550, 283, 285, 286

(56) References Cited

U.S. PATENT DOCUMENTS

4,054,010 A	10/1977	Shipman	451/159
4,066,943 A	1/1978	Roch	318/468
4,149,343 A	4/1979	Feldmeier	451/63
4,853,286 A	8/1989	Narimatsu et al.	428/343
4,941,293 A	7/1990	Ekhoff	451/342
5,056,971 A	10/1991	Sartori	409/201
5,173,863 A	12/1992	Martin	700/164
5,178,461 A	1/1993	Taniguchi	366/332
5,209,760 A	5/1993	Wiand	51/293
5,476,566 A	12/1995	Cavasin	

5,494,862 A	2/1996	Kato et al.	438/693
5,549,511 A	8/1996	Cronin et al.	451/281
5,567,503 A	* 10/1996	Sexton et al.	428/137
5,579,212 A	11/1996	Kato et al.	

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

EP	0776030 A2	5/1997
EP	0940219 A2	9/1999
EP	1050374 A2	11/2000
JP	61-152358 A	7/1986

(List continued on next page.)

OTHER PUBLICATIONS

Systems Dynamics, Inc. web page, www.sysdyn.com/expages/LMIS.htm, May 2, 2001, 2 pages.

GSI Lumonics WaferMark® SigmaXC Nd:YLF-Laser
Marking System, www.marwell.se/mis2/15wmsxc.html, May
5, 2001, 2 pages.

Norbert Maurer et al., *High Speed Laser Marking Pen-type
Nd: YAG Systems*, Semiconductor-Fabtech.com TAP
Resource, www.fabtech.org/features/tap/articles/02.309.html, May 2, 2001, pp. 1-6.

Primary Examiner—Joseph J. Hail, III

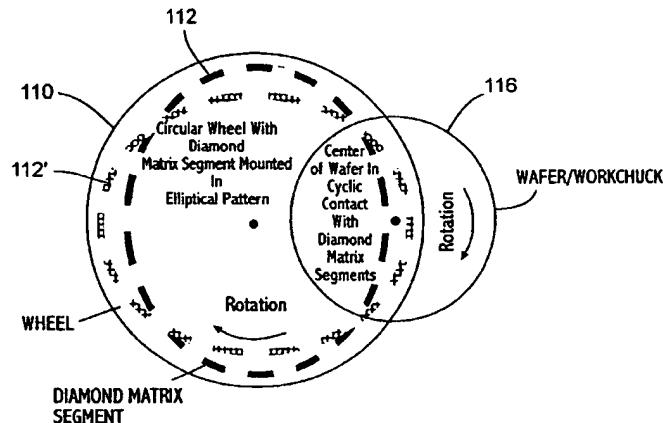
Assistant Examiner—David B. Thomas

(74) Attorney, Agent, or Firm—Townsend and Townsend
and Crew LLP

(57) ABSTRACT

The present invention provides exemplary methods, systems and apparatus that provide improved substrate characteristics after grinding operations by avoiding or reducing overgrind damage to the wafers. In one embodiment, a grinding apparatus (100) includes a first spindle (110) having an eccentric-shaped abrasive matrix (112) coupled thereto and a second spindle (116) adapted to hold a substrate (118) to be ground. The second spindle is offset from said first spindle such that the abrasive matrix passes through the substrate surface center (134) for only a portion of the time during grinding operations.

19 Claims, 8 Drawing Sheets



ECCENTRIC ABRASIVE WHEEL FOR WAFER PROCESSING

CROSS-REFERENCES TO RELATED APPLICATIONS

This application claims the benefit of the following U.S. Patent Applications, the complete disclosures of which are incorporated herein by reference:

U.S. Provisional Application No. 60/264,569 filed on Jan. 26, 2001;

U.S. patent application Ser. No. 09/808,790, entitled "Cluster Tool Systems and Methods for Processing Wafers," filed on Mar. 15, 2001; and

U.S. patent application Ser. No. 09/808,748, entitled "Cluster Tool Systems and Methods to Eliminate Wafer Waviness During Grinding," filed on Mar. 15, 2001.

BACKGROUND OF THE INVENTION

The present invention is directed to the processing of wafers, substrates or disks, such as silicon wafers, and more specifically to cluster tool systems, equipment and methods for processing wafers prior to device formation.

Wafers or substrates with exemplary characteristics must first be formed prior to the formation of circuit devices. In determining the quality of the semiconductor wafer, the flatness of the wafer is a critical parameter to customers since wafer flatness has a direct impact on the subsequent use and quality of semiconductor chips diced from the wafer. Hence, it is desirable to produce wafers having as near a planar surface as possible.

In a current practice, cylindrical boules of single-crystal silicon are formed, such as by Czochralski (CZ) growth process. The boules typically range from 100 to 300 millimeters in diameter. These boules are cut with an internal diameter (ID) saw or a wire saw into disc-shaped wafers approximately one millimeter (mm) thick. The wire saw reduces the kerf loss and permits many wafers to be cut simultaneously. However, the use of these saws results in undesirable waviness of the surfaces of the wafer. For example, the topography of the front surface of a wafer may vary by as much as 1-2 microns (μ) as a result of the natural distortions or warpage of the wafer as well as the variations in the thickness of the wafer across its surface. It is not unusual for the amplitude of the waves in each surface of a wafer to exceed fifteen (15) micrometers. The surfaces need to be made more planar (planarized) before they can be polished, coated or subjected to other processes.

Planarizing processes include lapping or grinding, followed by polishing steps. A lapping process, for example, may be performed to control thickness and remove bow and warp of the silicon wafer. The wafer is simultaneously lapped on both sides with an abrasive slurry in a lapping machine. The lapping process may involve one or more lapping steps with increasingly finer polishing grit. The lapping process, however, is slow and must be followed by careful cleaning and etching steps to relieve stresses before the wafer is polished. These additional steps cause the conventional method to be expensive and time-consuming. Also, the etching process employed after lapping is undesirable from an environmental standpoint, because the large amount of strong acids used must be disposed of in an acceptable way.

In another method, a grinding process replaces the lapping procedure. A first surface of the wafer is drawn or pushed against a hard flat holder while the second surface of

the wafer is ground flat. Current grinding technology uses an abrasive wheel with a circular shaped diamond segment (bit) pattern as shown in FIG. 1A. This practice, however, causes the center of the wafer to be in constant contact with the grind segments (FIG. 1B). The constant contact in the center of the wafer is believed to create excess grinding at the wafer center relative to the wafer edge. Such a result tends to cause greater subsurface damage near the wafer center. For these and other reasons, the above techniques are undesirable.

Additional deficiencies in the current art, and improvements in the present invention, are described below and will be recognized by those skilled in the art.

SUMMARY OF THE INVENTION

The present invention provides exemplary methods, systems and apparatus that provide improved substrate characteristics after grinding operations by avoiding or reducing overgrind damage to the wafers. In one embodiment, an apparatus for grinding a substrate according to the present invention includes a first spindle having an eccentric-shaped abrasive matrix coupled thereto and a second spindle adapted to hold a substrate to be ground. The second spindle is offset from the first spindle.

In one aspect, the grinder further comprises a rotation device for rotating the first and second spindles. In one aspect, the first and second spindles are adapted to rotate such that the abrasive matrix passes through a center of the substrate only a portion of the time during which the first spindle completes a 360 degree rotation.

Preventing constant abrasive contact with the wafer center is accomplished a number of ways in alternative embodiments. In one aspect, the first spindle has a circular shaped surface to which an eccentric-shaped abrasive matrix is coupled. In another aspect, the first spindle has an elliptical shaped surface. The abrasive matrix is coupled near an edge of the elliptical shaped surface. In a particular embodiment, the abrasive matrix comprises a diamond bit pattern, although other abrasive matrix may be used within the scope of the present invention.

In one aspect of the present invention, grinding systems and apparatus further include a translation device coupled to the first spindle and adapted to translate the first spindle in a back and forth motion, or side-to-side motion. Similarly, in one aspect the translation device is coupled to the second spindle and is adapted to translate the second spindle in a back and forth motion, or side-to-side motion. In a particular embodiment, both spindles are translated to further ensure the wafer center is not over ground or over stressed.

In one aspect, the eccentric-shaped abrasive matrix is selected from an elliptical shape and an oval shape. In another aspect, the eccentric-shaped abrasive matrix further comprises a random abrasive matrix pattern.

In one embodiment of the present invention, a substrate grinding apparatus includes a first spindle having an abrasive matrix coupled to a first spindle surface, and a second spindle adapted to hold a substrate to be ground. The first and second spindles have first and second axii of rotation, respectively. The abrasive matrix has a non-circular pattern.

In one aspect, the first and second axii of rotation are generally parallel, and the first spindle is offset from the second spindle. In another aspect, the first and second spindles are adapted to rotate such that the abrasive matrix passes through a center of the wafer or substrate only a portion of the time during which the first spindle completes a 360 degree rotation. Again, the abrasive matrix may comprise a random pattern abrasive matrix.

Exhibit B



US006514423B1

(12) United States Patent
Ng et al.

(10) Patent No.: US 6,514,423 B1
(45) Date of Patent: Feb. 4, 2003

(54) METHOD FOR WAFER PROCESSING

(75) Inventors: Kan-Yin Ng, Maryland Heights, MO (US); Brent Teasley, Silex, MO (US)

(73) Assignee: MEMC Electronic Materials, Inc., St. Peters, MO (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/507,811

(22) Filed: Feb. 22, 2000

(51) Int. Cl.⁷ B29B 29/02

(52) U.S. Cl. 216/38; 216/53; 216/89; 216/99

(58) Field of Search 216/2, 38, 52, 216/53, 88, 89, 99; 451/37

(56) References Cited

U.S. PATENT DOCUMENTS

4,054,010 A	10/1977	Shipman	51/55
4,588,473 A	5/1986	Hisatomi et al.	
5,429,711 A	7/1995	Watanabe et al.	216/52
5,447,890 A	9/1995	Kato et al.	437/249
5,509,850 A	4/1996	Morioka et al.	451/168
5,516,706 A	5/1996	Kusakabe	437/12
5,569,063 A	10/1996	Morioka et al.	451/296
5,766,065 A	6/1998	Hasegawa et al.	451/173
5,855,735 A	* 1/1999	Takada et al.	216/88
5,899,743 A	5/1999	Kai et al.	
5,928,066 A	7/1999	Hasegawa et al.	451/173

FOREIGN PATENT DOCUMENTS

EP	0 617 456 A2	9/1994
EP	0 764 976 A1	3/1997
JP	9-298172	11/1997
WO	WO 99/09588	2/1999

OTHER PUBLICATIONS

E. Mendel and P. Sullivan; Reduction of Grinding and Lapping Defects, IBM Technical Disclosure Bulletin, vol. 25, No. 9, Feb. 1983.

* cited by examiner

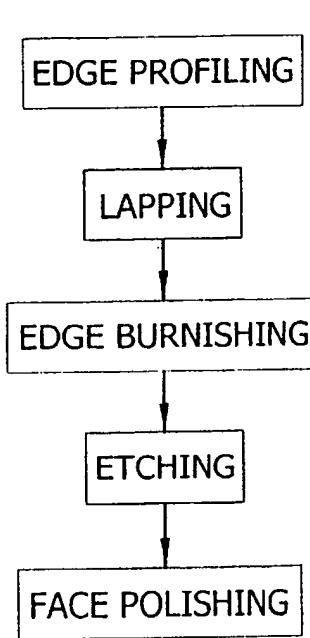
Primary Examiner—Allan Olsen

(74) Attorney, Agent, or Firm—Senniger, Powers, Leavitt & Roedel

(57) ABSTRACT

A method for processing a semiconductor wafer to reduce surface roughness. The wafer has two flat, opposite faces with a peripheral edge extending around a circumference of the wafer between the faces. The method includes, in the following order, the steps of burnishing the edge, and etching the edge. The step of burnishing is defined by a relative rubbing motion between the edge and an abrasive appliance to remove damage from the edge, the rubbing motion occurring free from any polishing solution or chemical slurry. The step of etching includes exposing the wafer to a liquid chemical etchant for a period of time to remove additional damage from the edge. The method may also include, before the other steps, a step of lapping at least one face of the wafer to remove semiconductor matter through a relative rubbing motion between the face and an abrasive lapping plate in the presence of an abrasive liquid slurry.

16 Claims, 1 Drawing Sheet



In yet another aspect, a method according to the present invention for processing a semiconductor wafer reduces surface roughness. The wafer has two flat, opposite faces and a peripheral edge extending around a circumference of the wafer between the faces. The method comprises, in the following order, the steps of lapping at least one face of the wafer to remove semiconductor matter through a relative rubbing motion between the face and an abrasive lapping plate in the presence of an abrasive liquid slurry. The peripheral edge of the wafer is burnished to remove semiconductor matter and embedded imperfections through a relative rubbing motion between the edge and an abrasive appliance, the rubbing motion occurring free from any polishing solution or chemical slurry. The wafer is etched to remove additional semiconductor matter and embedded imperfections by exposing the wafer to a liquid chemical etchant for a period of time.

Other objects and features of the present invention will be in part apparent and in part pointed out hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a flow diagram showing steps according to the prior art for processing a semiconductor wafer that include chemical-mechanical polishing of a peripheral edge; and

FIG. 2 is a flow diagram showing steps according to the present invention for processing the semiconductor wafer that include burnishing of the peripheral edge.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to the drawings and in particular to FIG. 2, a method for semiconductor wafer processing, including particularly a method for processing a peripheral edge of a wafer, is shown. The method smooths wafer surfaces and removes embedded imperfections to facilitate the installation of integrated circuit devices.

As is well known to those of ordinary skill in the art, a cylindrical, single crystal ingot of a semiconductor material, such as silicon, is commonly prepared using the so-called Czochralski process. In this process, polycrystalline silicon is melted in a crucible, a seed crystal is brought into contact with the molten silicon, and a single crystal silicon ingot is grown by slow extraction. The ingot is sliced, as by using a conventional inner diameter saw or wire saw apparatus. Each slice forms a thin, disk-shaped wafer having two flat, opposite facial surfaces and a peripheral edge extending around a circumference of the wafer between the faces. During the slicing operation, facial surfaces and the edge receive damage, including microcracks, chips, and roughness.

As shown on FIG. 2, the peripheral edge of the wafer is profiled. A grinding tool which carries abrasive material, such as diamond, grinds the edge to shape its contour. Sharp or square corners along the edge are rounded and a selected cross sectional profile is formed. The edge receives damage during this profiling operation, producing additional chips and roughness.

The wafer is lapped to remove semiconductor matter, improving uniformity of thickness and flatness. A conventional lapping operation uses an apparatus that simultaneously processes up to 25 wafers. The apparatus effects a relative rubbing motion between a set of rotating lapping plates and the face of the wafer in the presence of an abrasive liquid slurry, removing material and embedded damage by mechanical abrasion. Lapping may be totally or partially

replaced by grinding without departing from the scope of the present invention.

Following lapping, the peripheral edge of the wafer is burnished to remove semiconductor matter, reducing surface roughness and embedded imperfections. Burnishing comprises rubbing a suitable abrasive appliance along the edge, the rubbing motion occurring free from any polishing solution or chemical slurry. Preferably, the step of burnishing is done using an edge burnishing machine of the type shown in U.S. Pat. No. 5,509,850. In practice, a machine found useful is a model NME-68N edge burnisher manufactured by Mipox International Corporation, having offices in Hayward, Calif. In that machine, the wafer is rotatably held in a generally horizontal orientation by a vacuum chuck. The abrasive appliance is a thin flexible tape, about three inches wide, that is coated with abrasive grit or particles. Tape having grit of a specific size may be selected, with available sizes ranging from at least 0.5 to 30.0 microns. The magnitude of resulting edge roughness is directly related to the abrasive grit size.

The abrasive tape is threaded inside the burnishing machine on a head that may vibrate generally along the circumference of the wafer and simultaneously rotate transverse to the edge, about an axis generally tangential to the circumference. The tape is simultaneously fed through the head between reels on the machine. Rotation of the head permits the tape to engage and burnish the edge over a range of relative angles corresponding with the cross sectional profile shape of the edge, so that the entire edge is uniformly burnished. Typically, the head presses the tape against the edge and cycles in rotation from a nominal position where the tape is vertically oriented, perpendicular to the wafer, to positions about 68° in either direction away from vertical. Rotation of the head occurs simultaneously with its vibration and with wafer rotation about its center. A stream of liquid water is typically provided to cool the wafer and eliminate abraded material, but there is no slurry with chemically active agents. In other words, there is no chemical present which reacts with the semiconductor material to cause its removal. The step of burnishing may be repeated once or several times with tapes of sequentially smaller grit size to reduce the size of edge damage and improve smoothness.

After burnishing, the wafer is etched as shown on FIG. 2 to remove additional semiconductor matter and embedded imperfections. Typically, a liquid etchant comprises an aqueous solution of nitric acid, hydrofluoric acid, phosphoric acid, and an oxidizing agent that produces a chemical reaction with silicon. The reaction removes damaged surface layers to yield improved gloss and smoothness. The wafer is preferably immersed in a bath of etchant for a period of time ranging from about 1 minute to about 10 minutes, and more preferably for about 2 to 3 minutes. As is commonly known to one skilled in the art, it is preferable that the etchant be continuously mixed or agitated for the duration of the etching process. The wafer may be rotated while immersed in the etchant to promote uniform etching across the surfaces of the wafer, which is especially preferable if the wafer is supported during etching by a wafer carrier that obstructs any portion of the wafer from exposure to etchant. Other forms of etching may be employed without departing from the scope of the present invention.

After the step of etching, chemical-mechanical polishing on at least one face of the wafer is conducted by effecting a relative rubbing motion between the face and a polishing pad in the presence of a polishing solution or chemical slurry. Polishing is one of the more expensive and time consuming steps in wafer manufacturing. To maximize

Exhibit C



US006030485A

United States Patent [19]

Yamada

[11] Patent Number: 6,030,485

[45] Date of Patent: Feb. 29, 2000

[54] **METHOD AND APPARATUS FOR
MANUFACTURING A SEMICONDUCTOR
DEVICE**

[75] Inventor: Yutaka Yamada, Kawasaki, Japan

[73] Assignee: Fujitsu Limited, Kawasaki, Japan

[21] Appl. No.: 09/037,003

[22] Filed: Mar. 9, 1998

[30] Foreign Application Priority Data

Aug. 25, 1997 [JP] Japan 9-228547

[51] Int. Cl. 7 B32B 35/00

[52] U.S. Cl. 156/344; 156/154; 156/584;
438/759

[58] Field of Search 156/154, 344,
156/584; 29/426.1, 426.3, 426.4, 426.5,
426.6; 438/759

[56] References Cited

U.S. PATENT DOCUMENTS

5,268,065 12/1993 Grupen-Shemansky 156/154 X
5,476,566 12/1995 Cavasin 156/154 X
5,480,842 1/1996 Clifton et al. 438/464
5,840,614 11/1998 Sim et al. 438/464

FOREIGN PATENT DOCUMENTS

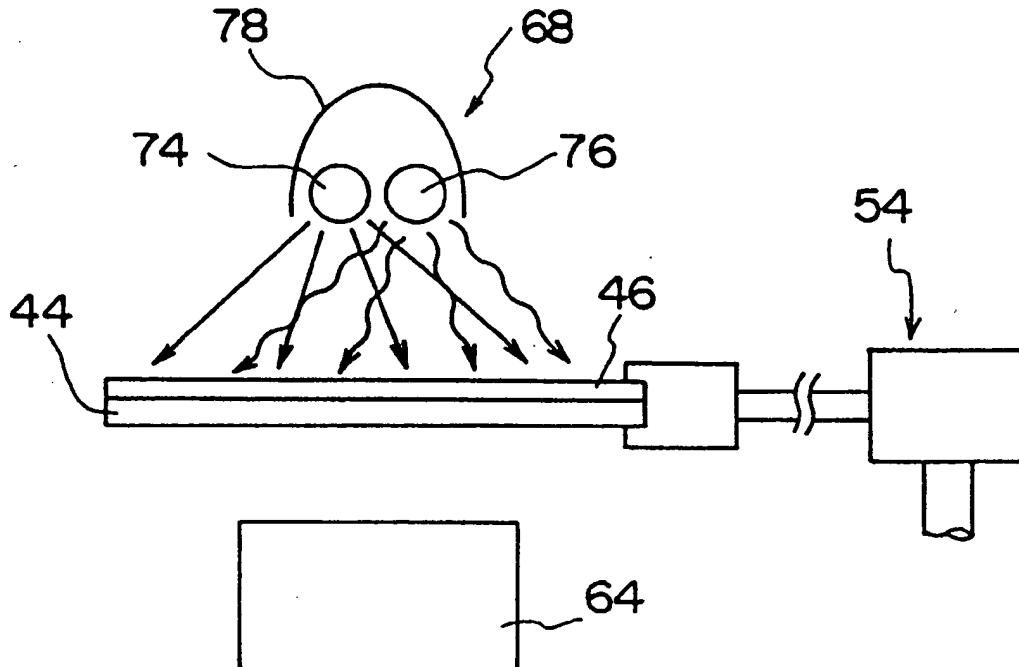
61-1037 1/1986 Japan 438/FOR 386

Primary Examiner—Mark A. Osele
Attorney, Agent, or Firm—Armstrong, Westerman, Hattori,
McLeland & Naughton

[57] ABSTRACT

An apparatus for manufacturing a semiconductor device includes a wafer grinding section which grinds a wafer fixed on an ultraviolet sensitive tape and a drying section which dries the wafer after the wafer is ground. The drying section includes an ultraviolet irradiation device irradiating the ultraviolet sensitive tape with ultraviolet rays.

9 Claims, 7 Drawing Sheets



1

**METHOD AND APPARATUS FOR
MANUFACTURING A SEMICONDUCTOR
DEVICE**

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to a method and an apparatus for manufacturing a semiconductor device, and particularly relates to a method and an apparatus for manufacturing a semiconductor device for implementing a wafer grinding process on a wafer fixed on an adhesive tape.

2. Description of the Related Art

A semiconductor manufacturing process includes a wafer process and a subsequent wafer grinding process. In the wafer process, semiconductor elements are formed on one surface (a front surface) of a wafer. In the wafer grinding process, the other surface (a back surface) of the wafer, without any semiconductor element, is ground so as to reduce a thickness of a wafer. However, it is difficult to handle the wafer with reduced thickness since the wafer may easily break.

Accordingly, a method and an apparatus for manufacturing a semiconductor device is required, which makes it easier to handle the wafer with reduced thickness and can prevent the breakage of the wafer.

Also, because the semiconductor manufacturing process is ever complex, more devices are required for manufacturing semiconductors. Therefore, there is a need for improving space efficiency of a semiconductor device manufacturing plant. Thus, further miniaturization of the apparatus for manufacturing semiconductors is also required.

Referring now to FIGS. 1-6, a method and an apparatus of the related art for manufacturing a semiconductor device will be described. FIG. 1 shows a prior device structure for a back grinding process that performs wafer grinding on the back surface of the wafer. FIGS. 2-6 show a method of implementing a prior back grinding process.

As shown in FIG. 1, in the prior back grinding process, the back grinding process is performed on a wafer 14 using a supply cassette 2, a storage cassette 4, a transfer machine 6, a wafer grinder 8, an ultraviolet (UV) irradiation device 10 and a remover 12. Hereinafter, each of the above devices will be described in its operation.

The supply cassette 2 is preloaded with the wafer 14 provided with an ultraviolet sensitive tape 16 (herein after referred to as a UV tape) on the front surface as shown in FIG. 2 (tape laminated). The transfer machine 6 extracts the wafer 14 provided with the UV tape 16 from the supply cassette 2 and transfers it to the wafer grinder 8.

The wafer grinder 8 is generally formed of a wafer grinding section 18 and a drying section 20. First, as shown in FIG. 3, the transfer machine 6 fixes the wafer 14 on a chuck table 28 provided in the wafer grinding section 18. The chuck table 28 is connected to a vacuum device so as to hold the wafer 14 on the chuck table 28 by vacuum. The wafer 14 is fixed on the chuck table 28 with the UV tape 16 placed at the bottom.

Subsequently, a grinding process (back grinding process) is performed until the wafer 14 has a required thickness. A grinding tool 22 comes into contact with the back surface (a surface with no element and provided with the UV tape) of the wafer 14 and then rotates to carry out this grinding process. In order to remove scraps and to cool the wafer 14, cleaning liquid is supplied to the surface subjected to the grinding process.

2

After being subjected to the grinding process at the wafer grinding section 18, the wafer 14 is transferred to the drying section 20 by the transfer machine 6. Then as shown in FIG. 4, the cleaning liquid is dried using a light source 24 such as a halogen lamp.

As described above, after the back grinding process and the drying process on the wafer 14 in the wafer grinder 8, the transfer machine 6 extracts the wafer 14 from the wafer grinder 8 and then transfers the wafer 14 to the UV irradiation device 10. As shown in FIG. 5, the UV tape 16 is irradiated with ultraviolet (UV) rays from an ultraviolet (UV) lamp 26.

A characteristic feature of an adhesive agent provided on the UV tape 16 is that it becomes stiff when irradiated with the ultraviolet rays. Thus by irradiating the UV tape 16 with the ultraviolet rays, the adhesive agent will become less adhesive. This facilitates the removal of the UV tape from the wafer 14.

As shown above, after irradiating the wafer 14 with the ultraviolet in the UV irradiation device 10, the transfer machine 6 extracts the wafer 14 from the UV irradiation device 10 and then transfers the wafer 14 to the remover 12. As shown in FIG. 6, the UV tape 16 is peeled off from the wafer 14 in the remover 12.

In the related art, the back grinding process is implemented on the wafer 14 using devices 2-12 and processes described above.

However, in the related art, devices such as the transfer machine 6, the wafer grinder 8, the UV irradiation device 10 and the remover 12 were required separately in order to perform the back grinding process. Also, there was a need for the transfer machine 6 in order to mount and extract the wafer 14 between each of devices 6-12.

Accordingly, it was necessary to provide a large number of devices 8-12 within a semiconductor manufacturing plant and to connect those devices 8-12 via a transfer machine 6. Therefore, there was a problem that a large installation space was needed within the plant.

Also, the transfer machine 6 mounts and extracts the wafer 14 between each device 2-12. Therefore, a considerable time is required between the extraction of the wafer 14 with the UV tape from the supply cassette 2 and the irradiation of the UV tape 16 at the UV irradiation device 10. This can cause a problem since the adhesiveness of the UV-sensitive adhesive agent provided on the UV tape may also change due to radiation from a fluorescent lamp.

Particularly, when a considerably long time is required before ultraviolet irradiation of the UV tape 16 as in the related art, the property of the adhesive agent will be greatly changed by a fluorescent lamp. Accordingly, the adhesive agent will not be sufficiently stiff when the UV tape 16 is irradiated by the ultraviolet in the UV irradiation device 10. This causes a problem that the adhesive agent may remain on the wafer 14 when peeling off the UV tape 16 from the wafer 14 by the remover 12.

Any residual adhesive agent on the wafer 14 will be inconvenient in the following manufacturing process for the semiconductor device. Therefore, in the related art, there was a need for a cleaning process after the removing process for removing any residual adhesive agent. This introduced an additional complexity to the process of manufacturing the semiconductor device.

SUMMARY OF THE INVENTION

Accordingly, it is a general object of the invention to provide a method and an apparatus for manufacturing a semiconductor device, which can satisfy the needs described above.

3

It is another and more specific object of the present invention to provide a method and an apparatus for manufacturing a semiconductor device which can positively peels off an ultraviolet sensitive tape (UV tape) from the wafer and can reduce the installation space requirement.

In order to achieve the above objects according to the present invention, an apparatus for manufacturing a semiconductor device includes:

- a wafer grinding section which grinds a wafer fixed on an ultraviolet sensitive tape; and
- a drying section which dries the wafer after the wafer is ground,
- wherein the drying section includes an ultraviolet irradiation device irradiating the ultraviolet sensitive tape with ultraviolet rays.

In the apparatus described above, the wafer grinding section implements the wafer grinding process to the wafer fixed to the UV tape so as to grind the wafer to a required thickness. During the wafer grinding process, the wafer will not be damaged since the wafer is protected by the UV tape fixed thereon. Subsequently, the drying process is implemented on the wafer in order to dry the cleaning liquid used during the wafer grinding.

Also, the ultraviolet irradiation device for irradiating the UV tape with ultraviolet rays is integrated in the drying section. Thereby the ultraviolet-sensitive adhesive agent provided on the UV tape may become stiff at an early stage after the wafer grinding process. Since the wafer grinding section and the drying section are provided within the same manufacturing apparatus, light such as light from a fluorescent lamp may not act on the adhesive agent provided on the UV tape.

Accordingly, the adhesive agent does not remain on the wafer when peeling off the UV tape from the wafer. Therefore, a cleaning process for removing the residual adhesive agent is no longer necessary. Thus, the semiconductor device manufacturing process may be simplified.

Further, the ultraviolet irradiation device is integrated in the drying section. This miniaturizes the apparatus for manufacturing the semiconductor device as compared to the prior manufacturing apparatus, which included separate ultraviolet irradiation devices. Thereby, an installation space of the manufacturing apparatus may be reduced within a semiconductor device manufacturing plant.

It is still another object of the invention to provide an apparatus for manufacturing a semiconductor device, which can implement the drying process and the ultraviolet irradiation process simultaneously and can improve the efficiency of semiconductor device manufacturing process.

In order to achieve the above object, the ultraviolet irradiation device is provided so as to oppose a predetermined wafer drying position within the drying section.

It is yet another object of the invention to provide an apparatus for manufacturing a semiconductor device, which can improve the efficiency of the drying process.

In order to achieve the above object, the drying section further includes a chuck table mounting the wafer, the chuck table having a surface area smaller than that of the wafer. Also, the drying section further includes a holder that holds the wafer at a predetermined distance above the chuck table during the drying process.

It is yet another object of the invention to provide an apparatus for manufacturing a semiconductor device which can transfer the wafer without exposing the wafer to light such as light from a fluorescent lamp adversely acting on the adhesive agent provided on the UV tape.

In order to achieve the above object, the apparatus for manufacturing a semiconductor further includes a transfer

4

machine that automatically transfer the wafer from the wafer grinding section to the drying section within the apparatus.

It is yet another object of the invention to provide a method and an apparatus for manufacturing a semiconductor device which can reduce the time required for the manufacturing process as compared to the related art which implements each process separately.

In order to achieve the above object, the ultraviolet irradiation device includes both an ultraviolet lamp and a halogen lamp. Also, a method of manufacturing a semiconductor using the above described apparatus for manufacturing a semiconductor device includes the step of irradiating the ultraviolet sensitive tape with ultraviolet rays while drying the wafer.

15 It is yet another object of the invention to provide a method and an apparatus for manufacturing a semiconductor device, which can reduce an installation space of the manufacturing apparatus within a semiconductor device manufacturing plant, when compared to the related art.

20 In order to achieve the above object, the drying section further includes a remover which peels off the ultraviolet sensitive tape from the wafer, the ultraviolet sensitive tape having been irradiated with ultraviolet rays by the ultraviolet irradiation device and having become stiff. Also, the method 25 of manufacturing a semiconductor further includes the step of peeling off the ultraviolet sensitive tape from the wafer after the irradiation step.

Other objects and further features of the present invention will be apparent from the following detailed description 30 when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagrammatic view of a device used in a back grinding process of the related art.

35 FIG. 2 is a cross sectional diagram of a wafer before a wafer grinding process.

FIG. 3 is a cross sectional diagram of a wafer under a wafer grinding process.

40 FIG. 4 is a diagram showing an operation of the drying section of the related art.

FIG. 5 is a diagram showing an operation of the UV radiation device of the related art.

45 FIG. 6 is a diagram showing an operation of the remover of the related art.

FIG. 7 is a diagrammatic view of a semiconductor device manufacturing apparatus of an embodiment of the present invention.

50 FIG. 8 is a cross sectional diagram of a wafer before a wafer grinding process according to the present invention.

FIG. 9 is a diagram showing an operation of the wafer grinding section of the present invention.

55 FIG. 10 is a diagram showing an operation of the drying section of the present invention.

FIG. 11 is a diagram showing an operation of the remover of the present invention.

60 FIG. 12 is a diagram showing a second operation of the remover of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following, a principle and an embodiment of the present invention will be described with reference to the accompanying drawings.

65 FIG. 7 shows a semiconductor device manufacturing apparatus 30 of an embodiment of the present invention.